FIG. **1**A is a schematic diagram illustrating a device including a Zener diode with a transistor according to an aspect of the present disclosure. The device **100** includes a Zener diode **110** and a "normally on" field effect transistor **130** that provides a constant current with respect to an input voltage, such as a drain voltage. As shown in FIG. **1**A, the anode of the Zener diode **110** is connected to the drain of the transistor **130**. The transistor **130** may be a depletion-mode transistor, which is a normally ON device and can increase or reduce its drain current by the gate potential. It shuts off the drain current by either or both gate and source potential. By way of example and not by way of limitation, the transistor **130** may alternatively be a junction gate field-effect transistor (JFET). The Zener voltage of the Zener diode **110** is used to control the voltage input to the transistor **130**. When the input voltage is lower than the breakdown voltage of the Zener diode **110**, the transistor **130** is disabled and there no current flows through it. When the input voltage is higher than the breakdown voltage, the transistor **130** conducts current. While FIG. **1**A shows only one Zener diode **110** is connected to a transistor **130**, it is noted that two or more Zener diodes can be connected in series as shown in FIG. **2**A to add up the Zener voltages as the detection voltage or start-up voltage for turning on the connected transistor **130**.

FIG. **1**B is a cross-sectional view illustrating portions of a device integrating a Zener diode with a transistor in a single chip according to one embodiment of the present disclosure. The device **100** includes a substrate **102** of a first conductivity type semiconductor (e.g., P substrate). The substrate **102** may be doped with a P-type dopant such as boron. An (optional) epitaxial layer **104** of the first conductivity type (e.g., P type epitaxial layer) is formed over the P-type substrate **102**. In one example, the epitaxial layer **104** may be formed by an epitaxial growth process as known in the art. The substrate **102** and the epitaxial layer **104** is lightly doped. In some implementation, they may have a doping concentration that is in a range from about 10^{14}/centimeter^3 to about 10^{16}/centimeter^3. The thickness of the epitaxial layer **104** may be in a range from about 2 microns to about 10 microns.

The Zener diode **110** and the depletion-mode transistor **130** are formed in the P-type epitaxial layer **104** over the P-type substrate **102**. With respect to the Zener diode **110**, an N-type well **112** and a P-type well **122** may be provided in the P-type epitaxial layer **104**. An N+ region **114** serves as the cathode of the diode is encompassed in the N-type well **112**. A P+ region **124** serves as the anode of the diode is encompassed in a P-type body region **126** in the P-type well **122**. These regions may be formed by ion implantation process known in the art. The doping concentrations of the N-type well **112** and the P-type well **122** determine the turn on voltage for the Zener diode **110**. The N+ region **114** is more heavily doped than the N-type well **112**. A slight gap of, e.g., a few $1/10^{ths}$ of a micron to a few microns between the N-type well **112** and P-type well **122** can increase the breakdown voltage. In some implementation, the N+ region **114** has a doping concentration that is in a range from about 10^{19}/cm^3 to about 10^{21}/cm^3 and the N-type well **112** has a doping concentration of about 10^{16}/cm^3 to about 10^{18}/cm^3. In addition, the P+ region **124** is doped heavier than the P-type body region **126** and the P-type well **122**. The P+ region is almost saturated. In some implementations, the P+ region **124** may have a doping concentration that is in a range from about 10^{19}/cm^3 to about 10^{20}/cm^3. The doping concentration of the P-type body region **126** and the P-type well **122** is about 10^{16}/cm^3 to about 10^{18}/cm^3.

With respect to the transistor **130**, a P-type well **132** as the body of the transistor **130** is provided in the P-type epitaxial layer **104**. P+ body pickup and N+ source regions are formed in the body **132**. The P+ body pickup may have a doping concentration that is in a range from about 10^{19}/cm^3 to about 10^{20}/cm^3 and the N+ source may have a doping concentration of about 10^{19}/cm^3 to about 10^{21}/cm^3. In addition. The P-type well **132** is doped heavier than the P-type substrate **102**. A layer of polysilicon **134** serving as the gate of the transistor **130** is provided over the top surface of the P-type epitaxial layer **104**. The gate **134** is electrically isolated from the epitaxial layer **104** with a gate insulator layer, e.g., an oxide. In addition, the device may include field oxide (not shown), e.g., over active areas for the gate and N+/P+ implant regions, as is conventionally done. For the sake of clarity and simplicity, regions of field oxide have been omitted. However, devices that include field oxide are within the scope of the present disclosure.

A high voltage N-type well (HVNW) **138** is provided in the P-type epitaxial layer **104** to provide drain extension area. The lightly doped HVNW **138** has a doping concentration that is in a range from about 10^{15}/cm^3 to about 10^{17}/cm^3. A depletion implant layer **135** is located under the gate and over portions of the P-well **132** and the HVNW **138**. The depletion layer, **135**, makes the MOS FET **130** a normally on device. The on state can be turned off by controlling either gate or source potential with respect to the body potential. A heavily doped N+ region **136** encompassed in the HVNW **138** serves as the drain of the transistor **130**.

In addition, a junction area **150** including a punch through stop **152** is disposed between the diode **110** and the transistor **130**. The punch through stop is basically a region of the substrate **102** and epitaxial layer **104** that is less heavily P-type doped than, e.g., the P-well **122** and P$^+$ regions **124**, **126**. At the edges of the junction area **150**, isolation structures are provided. The punch through voltage of the device can be adjusted by adjusting the width of the punch through stop **152**. Preferably the punch though voltage is greater than the turn on voltage of the Zener diode **110**. If the punch through voltage is "lower" than Zener breakdown voltage, the Zener diode **110** would conduct current to the transistor **130** before the breakdown. This would render the Zener non-functional

In order to integrate the Zener diode **110** and transistor **130** into the same substrate devices according to aspects of the present disclosure include an isolation structure configured to act as a punch through stopper between anode of Zener diode and the substrate **102**. An isolation structure may include an N-type buried layer (NBL) **106**, an N-type well **108** on top of the NBL **106**, and a high voltage N-well (HVNW) **109** over the N-type well **108**. The doping concentration for the HVNW **109** may be in a range from about 10^{15}/cm^3 to about 10^{17}/cm^3. The NBL **106** is formed between the P-type substrate **102** and the P-type epitaxial layer **104**. The NBL **106** stops punch through from the P-well **122** or P-body region **126** to the P-type substrate **102**. As shown in FIG. **1**B, the NBL **106** is formed in the diode region and the edge of the junction area **150** to relax electrical field. A similar N-well **108** and an (optional) NBL **137** may be formed under the doped region **136** that acts as the drain of the transistor **130**. The NBL **137** may be omitted, if the electric field at the edge of the transistor **130** does not have to be relaxed.

For a very high voltage device, (e.g., >500V) the NBL **137** helps relax the field, but lower voltage device may not need it.